IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

DONALD C. ABBOTT ET AL.

Serial No. 09/525,105 (TI-28098)

Filed March 14, 2000

For: SEMICONDUCTOR CIRCUIT ASSEMBLY HAVING PLATED LEADFRAME INCLUDING GOLD SELECTIVELY COVERING AREAS TO BE SOLDERED

Art Unit 2826

Examiner Alexander O. Williams

Customer No. 23494

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Jay M. Cantor, Reg. No. 19,906

Sir:

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of claims 1 to 13 and 23 to 26, all of the rejected claims. No claims have been allowed, claims 14 to 16 have been canceled and claims 17 to 22 have been withdrawn from consideration. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was not filed after final rejection.

SUMMARY OF INVENTION

The invention relates to a leadframe (100, 301) for use with packaged integrated circuit chips and the packaged chip. The leadframe includes thereon gold (106, 106a, 313) selectively plated on segments of the leadframe intended for solder attachment. The leadframe can have a chip mount pad ((302) and a plurality of lead segments (305). The leadframe base is preferably made of copper or copper alloy, preferably with a first layer of nickel deposited on the copper or copper alloy, preferably with a layer of an alloy of nickel and palladium on the first nickel layer and preferably with a second layer of nickel on the alloy layer. The second nickel layer is deposited to be suitable for bending of the lead segments, wire bonding, and solder attachment. A layer of palladium is preferably deposited to be suitable for protecting the nickel surface for wire bonding and solderability, and for adhesion to molding compound and preferably gold is selectively plated on segments of the leadframe intended for solder attachment. The gold layer preferably has a thickness in the range from 2 to 5 nm, the first nickel layer preferably has a thickness in the range from 50 to 150 nm, the alloy layer preferably has a thickness

in the range from 50 to 150 nm, the second nickel layer preferably has a thickness in the range from 1000 to 3000 nm, the palladium layer preferably has a thickness in the range from 25 to 75 nm and the copper or copper alloy base preferably has a thickness between about 100 and 250 μm. The solder attachment preferably includes solder materials selected from a group consisting of tin/lead, tin/indium, tin/silver, tin/bismuth and conductive adhesive compounds. The leadframe preferably includes an iron-nickel alloy or invar base, selectively plated with gold. The layer of nickel preferably has a thickness in the range of about 500 nm to about 3000 nm, the palladium layer preferably has a thickness in the range of about 10 nm to about 30 nm and the gold preferably has a thickness in the range of about 6% to about 50 % of the thickness of the palladium layer.

ISSUES

The issues on appeal are as follows:

1. Whether claim 1 is anticipated by Lee et al. (U.S. 6,232,651) under 35 U.S.C. 102(e).

2. Whether claim 1 is anticipated by Hashizume (U.S. 5,946,556) under 35 U.S.C. 102(b).

3. Whether claims 2 to 13, 15 and 23 to 26 are patentable under 35 U.S.C. 103(a) over Abbott (U.S. 6,245,448) in view of Akino et al. (Japanese Patent Application No. 2000-77593).

4. Whether claims 2 to 13, 15 and 23 to 26 are patentable under 35 U.S.C. 103(a) over Abbott (U.S. 6,245,448) in view of Akino et al. (Japanese Patent Application No. 2000-77593) further in view of Hashizume (U.S. 5,946,556).

GROUPING OF CLAIMS

The claims do not stand or fall together for reasons set forth hereinbelow under ARGUMENT.

ARGUMENT

ISSUE 1

Claim 1 was rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. (U.S. 6,232,651). The rejection is without merit on its face.

The subject application bears a priority date of March 19, 1999 based upon provisional application 60.125,304. This date is prior to the filing date of Lee et al. Accordingly, Lee et al. is not available as a reference in this application.

ISSUE 2

Claim 1 was rejected under 35 U.S.C. 102(b) as being anticipated by Hashizume (U.S. 5,946,556). The rejection is without merit.

The Examiner refers to column 10, lines 26 to 34 as disclosing that which is claimed in claim 1, namely a leadframe and gold selectively plated on segments of the leadframe for solder attachment. The section of Hashizume referred to in the final rejection nowhere mentions selectivity. The practice in the prior art was to coat the entire leadframe rather than to be selective. Nowhere in this section of Hashizume is selectivity of plating area anywhere discussed or even hinted at and plating of the die pad and lead fingers results from plating of the entire surface as was the case in the prior art. It follows that the only basis for injection selectivity into Hashizume results from an initial reading of the subject disclosure.

ISSUE 3

Claims 2 to 13, 15 and 23 to 26 were rejected under 35 U.S.C. 103(a) as being unpatentable over Abbott (U.S. 6,245,448) in view of Akino et al. (Japanese Patent Application No. 2000-77593). The rejection is without merit on its face.

Abbott is assigned to the assignee of the subject application and is copending therewith. Accordingly, Abbott is not available as a reference under 35 U.S.C. 103(a) in view of 35 U.S.C.103(c).

ISSUE 4

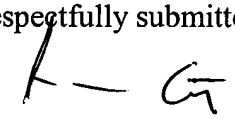
Claims 2 to 13, 15 and 23 to 26 were rejected under 35 U.S.C. 103(a) as being unpatentable over Abbott (U.S. 6,245,448) in view of Akino et al. (Japanese Patent Application No. 2000-77593) further in view of Hashizume (U.S. 5,946,556). The rejection is without merit on its face.

Abbott is assigned to the assignee of the subject application and is copending therewith. Accordingly, Abbott is not available as a reference under 35 U.S.C. 103(a) in view of 35 U.S.C.103(c).

CONCLUSIONS

For the reasons stated above, an arguments of the merits of the rejection is not required other than Issue 2 is not required. Accordingly, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,



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APPENDIX

The claims on appeal read as follows:

1. A leadframe for use with packaged integrated circuit chips comprising:

gold selectively plated on segments of said leadframe intended for solder attachment.

2. A leadframe for use with packaged integrated circuit chips having a chip mount pad and a plurality of lead segments, comprising:

a leadframe base made of copper or copper alloy;

a first layer of nickel deposited on said copper or copper alloy;

a layer of an alloy of nickel and palladium on said first nickel layer;

a second layer of nickel on said alloy layer, said second nickel layer deposited to be suitable for bending of said lead segments, wire bonding, and solder attachment;

a layer of palladium, said palladium layer deposited to be suitable for protecting the nickel surface for wire bonding and solderability, and for adhesion to molding compound; and

gold selectively plated on segments of said leadframe intended for solder attachment.

3. The leadframe according to Claim 2 wherein said gold layer has a thickness in the range from 2 to 5 nm.

4. The leadframe according to Claim 2 wherein said first nickel layer has a thickness in the range from 50 to 150 nm.

5. The leadframe according to Claim 2 wherein said alloy layer has a thickness in the range from 50 to 150 nm.

6. The leadframe according to Claim 2 wherein said second nickel layer has a thickness in the range from 1000 to 3000 nm.

7. The leadframe according to Claim 2 wherein said palladium layer has a thickness in the range from 25 to 75 nm.

8. The leadframe according to Claim 2 wherein said copper or copper alloy base has a thickness between about 100 and 250 μm.

9. The leadframe according to Claim 2 wherein said solder attachment comprises solder materials selected from a group consisting of tin/lead, tin/indium, tin/silver, tin/bismuth and conductive adhesive compounds.

10. The leadframe according to Claim 1 wherein said leadframe comprises an iron-nickel alloy or invar base, selectively plated with gold.

11. A packaged semiconductor device comprising:

a leadframe comprising a chip mount pad for an integrated circuit chip and a plurality of lead segments having their first end near said mount pad and their second end remote from said mount pad;

said leadframe having a first surface layer of nickel, a layer of an alloy of nickel and palladium, a second layer of nickel, and a layer of palladium;

said leadframe further having gold selectively plated on segments of said leadframe intended for solder attachment;

an integrated circuit chip attached to said mount pad; and

bonding wires interconnecting said chip and said first ends of said lead segments.

12. The device according to Claim 11 wherein said bonding wires are selected from a group consisting of gold, copper, aluminum and alloys thereof.

13. The device according to Claim 11 wherein the bonding wire contacts to said first ends of said lead segments comprise welds made by ball bonds, stitch bonds, or wedge bonds.

23. A packaged semiconductor device, comprising:

a leadframe comprising a chip mount pad for an integrated circuit chip and a plurality of lead segments;

said leadframe having a layer of nickel and a layer of palladium covering said chip mount pad and said plurality of lead segments, and gold selectively plated on portions of said lead segments intended for solder attachment;

an integrated circuit chip attached to said mount pad; and

bonding wires interconnecting said chip and said first ends of said lead segments.

24. A packaged semiconductor device, comprising:

a leadframe comprising a chip mount pad for an integrated circuit chip and a plurality of lead segments;

said leadframe having a layer of nickel and a layer of palladium covering said chip mount pad and said plurality of lead segments, and gold selectively plated on portions of said lead segments intended for solder attachment, wherein said layer of palladium has a thickness in the range of about 0.03% to about 6% of a thickness of said nickel layer;

an integrated circuit chip attached to said mount pad; and

bonding wires interconnecting said chip and said first ends of said lead segments.

25. The packaged semiconductor device of Claim 24, wherein said layer of nickel has a thickness in the range of about 500 nm to about 3000 nm and said palladium layer has a thickness in the range of about 10 nm to about 30 nm.

26. The packaged semiconductor device of Claim 24, wherein said gold has a thickness in the range of about 6% to about 50 % of said thickness of said palladium layer.